

7

AMENDMENTS TO THE DRAWINGS:

Figures 1 and 3 are amended to correct a minor spelling error (particularly, at reference numeral 8, the designation "DIGIT LINE." The Examiner respectfully is requested to acknowledge and approve the corrected drawings attached herewith.

Attachments: Replacement Sheets (2)
Annotated Sheets Showing Changes (2)

DIGIT

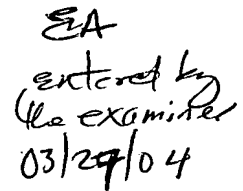


Fig. 2 is a block diagram of a memory system. It includes an **INPUT CIRCUIT** (1) connected to a **YDC** (2). The **YDC** (2) is connected to a **6 WORD LINE** (6). The **6 WORD LINE** (6) is connected to a **XDC** (3). The **XDC** (3) is connected to a **P1** (10b) block. The **P1** (10b) block is connected to a **D0** block. The **D0** block is connected to a **D1** block. The **D1** block is connected to an **OUTPUT CIRCUIT** (7). The **OUTPUT CIRCUIT** (7) is connected to **TO OUTSIDE CIRCUIT**. The **OUTPUT CIRCUIT** (7) is also connected to an **ECC OPERATION CIRCUIT** (4). The **ECC OPERATION CIRCUIT** (4) is connected to the **INPUT CIRCUIT** (1) and the **YDC** (2).

DIGIT

← A
extend by
the examiner
03/27/04



FIG. 4





FIG. 1

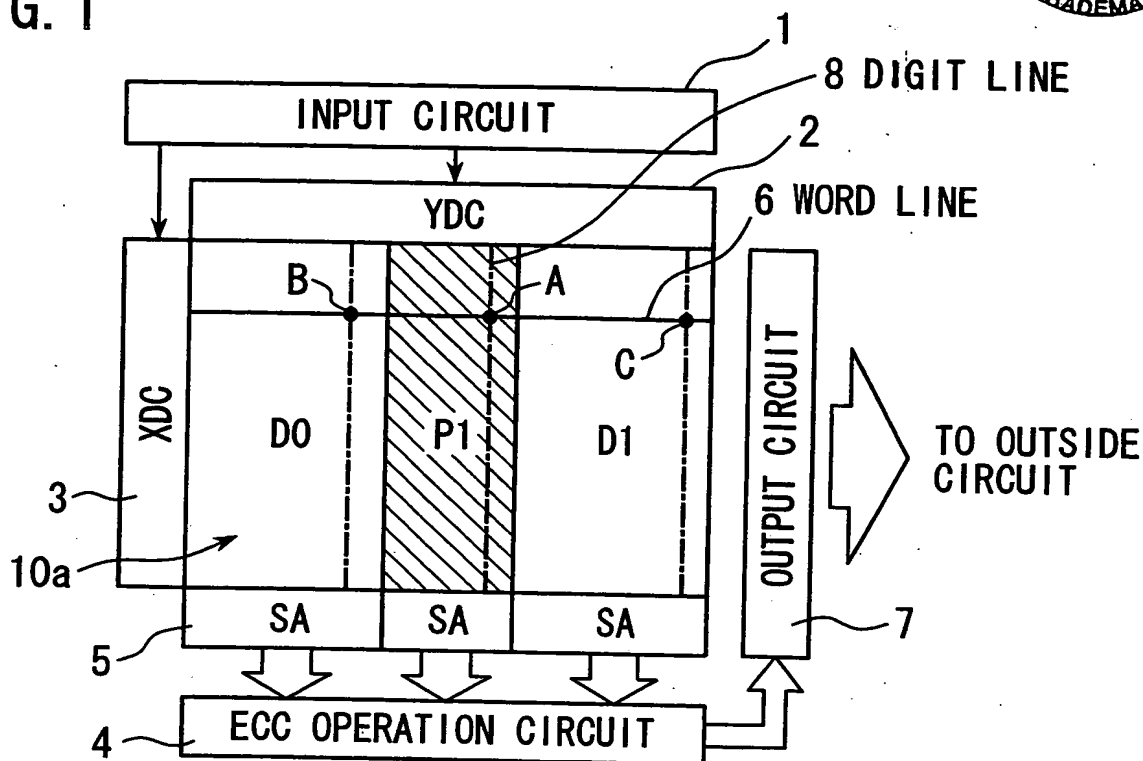


FIG. 2

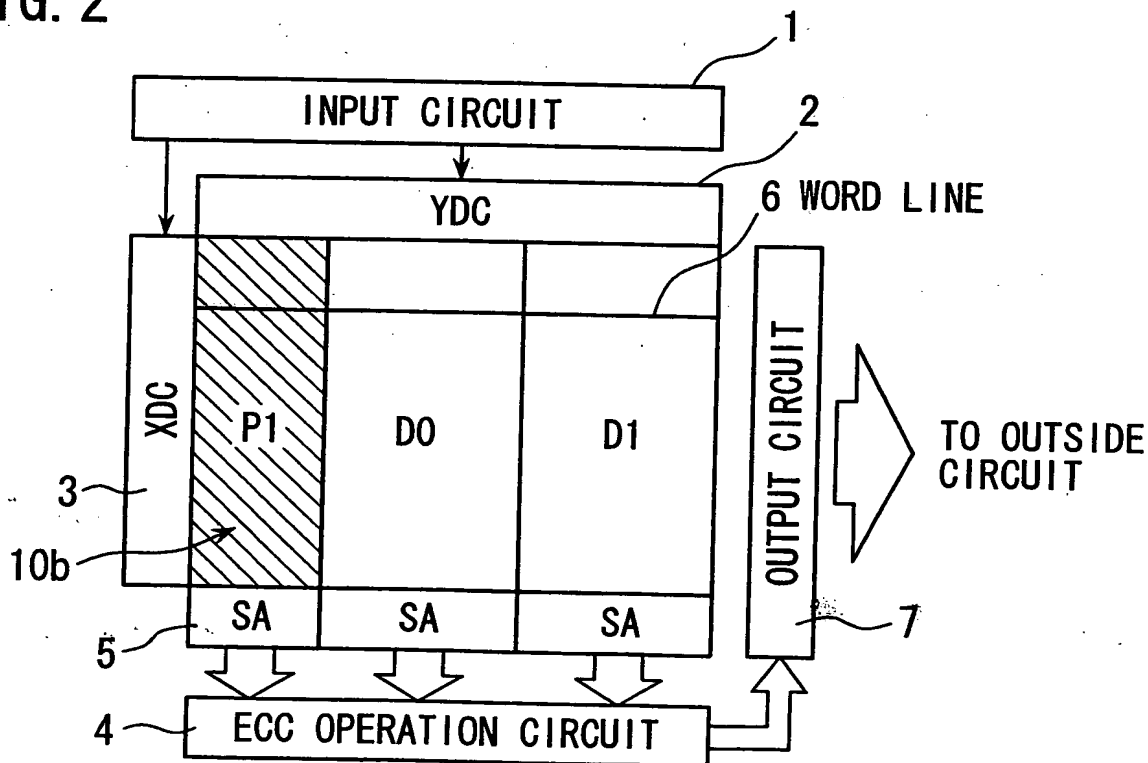
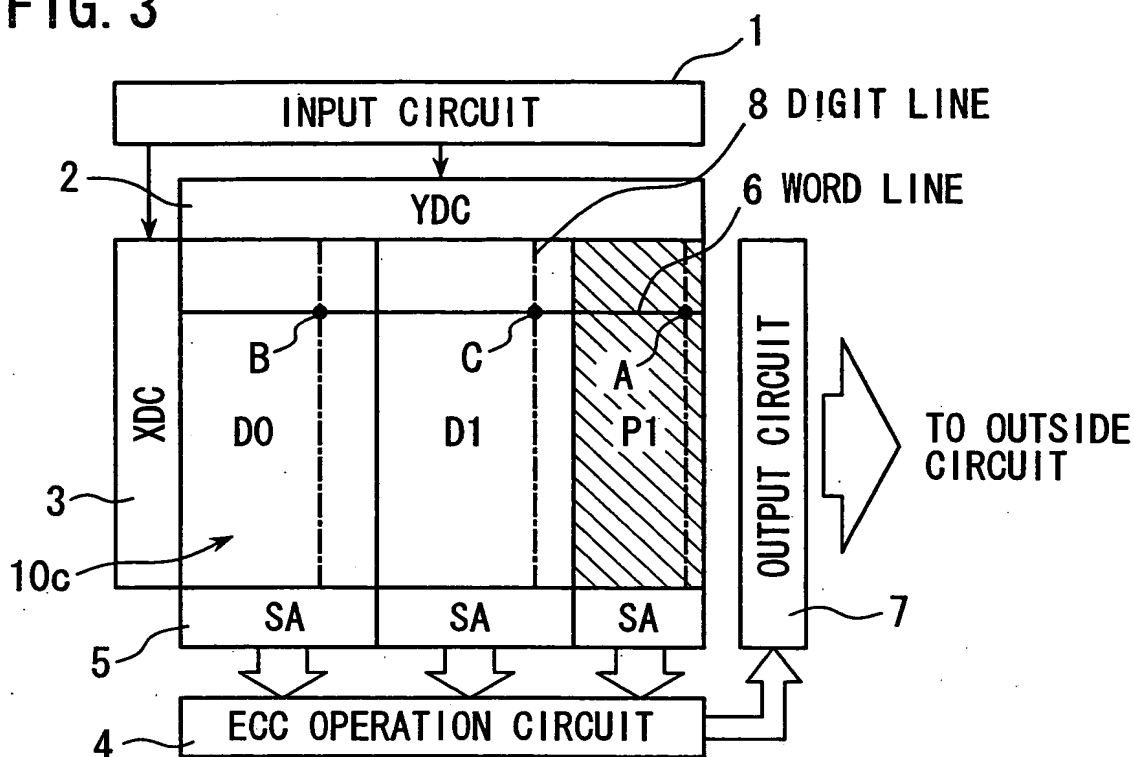


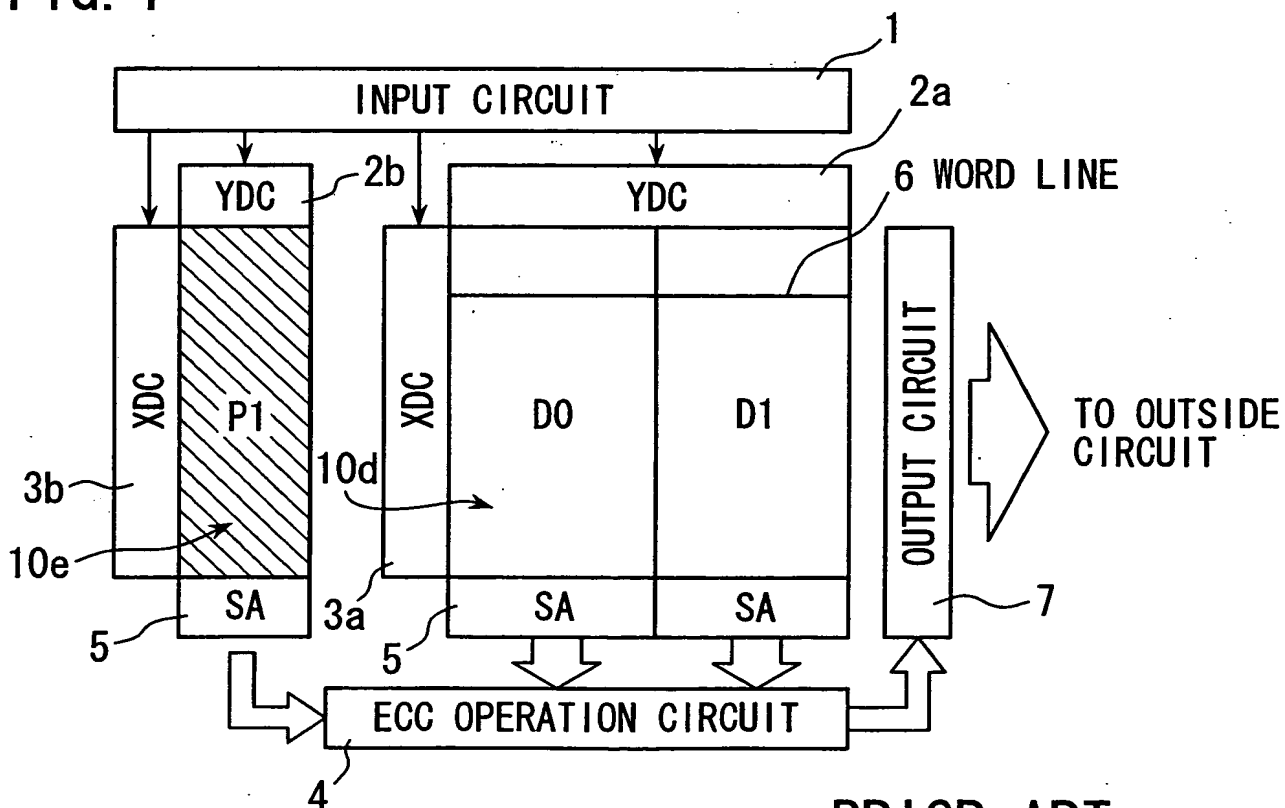


FIG. 3



PRIOR ART

FIG. 4



PRIOR ART